

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1 (withdrawn). A method of manufacturing a printed wiring board (81), comprising the steps of:

preparing an insulator substrate (1a) having first and second principal surfaces opposite to each other;

forming a first metal foil (82) on said first principal surface;

temporarily fixing a thermosetting resin film (84) to said second principal surface with said thermosetting resin film brought into contact with said second principal surface;

drilling, with said thermosetting resin film temporarily fixed to said second principal surface, a through hole (86) simultaneously in said first metal foil, said insulator substrate, and said thermosetting resin film so that said through hole extends in a direction substantially perpendicular to said first and said second principal surfaces;

simultaneously heating and vacuum-pressing, with a second metal foil (87) brought into contact with said thermosetting resin film after said drilling step, said first metal foil, said insulator substrate, said thermosetting resin film, and said second metal foil to obtain an intermediate printed wiring

board in which a bottom (92) of said through hole is covered with said second metal foil and in which the bottom of said through hole has a corner provided with a corner rounded portion (93) formed by said thermosetting resin film so as to protrude from said corner; and

forming a metal plating layer (95) on said first and said second metal foils of both sides of said intermediate printed wiring board, on an inner wall of said through hole, on said corner rounded portion, and on an exposed surface of said second metal foil exposed through the bottom of said through hole to obtain a final printed wiring board provided with interlayer connection.

2 (original). An interlayer connection printed wiring board (81) obtained by the steps of:

preparing an insulator substrate (1a) having first and second principal surfaces opposite to each other;

forming a first metal foil (82) on said first principal surface;

temporarily fixing a thermosetting resin film (84) to said second principal surface with said thermosetting resin film brought into contact with said second principal surface;

drilling, with said thermosetting resin film temporarily fixed to said second principal surface, a through hole (86) simultaneously in said first metal foil, said insulator

substrate, and said thermosetting resin film so that said through hole extends in a direction substantially perpendicular to said first and said second principal surfaces;

simultaneously heating and vacuum-pressing, with a second metal foil (87) brought into contact with said thermosetting resin film after said drilling step, said first metal foil, said insulator substrate, said thermosetting resin film, and said second metal foil to obtain an intermediate printed wiring board in which a bottom (92) of said through hole is covered with said second metal foil and in which the bottom of said through hole has a corner provided with a corner rounded portion formed by said thermosetting resin film so as to protrude from said corner; and

forming a metal plating layer (95) on said first and said second metal foils of both sides of said intermediate printed wiring board, on an inner wall of said through hole, on said corner rounded portion, and on an exposed surface of said second metal foil exposed through the bottom of said through hole.

3 (currently amended). A printed wiring board (81) including:

an insulator substrate (1a) having a first principal surface and a second principal surface opposite to said first principal surface; and

a first metal foil (82) formed on said first principal surface; and

~~a first metal layer~~ a second metal foil (87) formed on said second principal surface;

said insulator substrate and said first metal foil having a through hole (86) which is formed ~~therein~~ in said insulator substrate and said first metal foil and extends in a direction substantially perpendicular to said first and said second principal surfaces so that a part of a surface of said ~~first metal layer~~ second metal foil is exposed as an exposed surface through a bottom (92) of said through hole, the bottom of said through hole having a corner provided with a corner rounded portion (93) formed by a thermosetting resin film so as to protrude from said corner;

said printed wiring board comprising a ~~second metal layer~~ metal plating layer (95) formed on said first ~~principal surface~~ of said insulator substrate and said second metal foils, on an inner wall of said through hole, on said corner rounded portion, and on said exposed surface of the ~~first metal layer~~ second metal foil.

Amendments to the Drawing:

The attached sheets of drawing show proposed changes of the crosshatching of electrical insulation (resin) parts 9, 19, 20, 100, 120, and 130, as well as of metal part 1b, both in accordance with MPEP 608.02. At the same time, crosshatching of dry films 23 and 97 was omitted since these parts are not in section. Upon receiving the Examiner's approval, applicants will submit a formal drawing showing these changes.

Remarks/Arguments

The rejection of claim 2 under 35 U.S.C. 112 is not understood. As the law cited by the Examiner shows, "product-by-process" claims are **not** "indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention." All the case law indicates is that the method of making the product is not germane to the issue of patentability of the product. In other words, as stated in **In re Thorpe et al**, 227 USPQ 964, "If the product in a product-by-process claim is the same as or obvious from a product in the prior art, the claim is unpatentable." Thus, such claims are not excluded by Sec. 112 but their patentability cannot be argued on the basis of the method steps but it must be shown that the **product** differs patentably from the prior art product.

The rejection of claim 2 under 35 U.S.C. 102(e) as being anticipated by Uchikawa et al, cited, is respectfully traversed. In the first place, applicants note that they enjoy the priority date of February 28, 2001 under 35 U.S.C. 119, which precedes the U. S. filing date of the cited patent. Therefore, Uchikawa et al is not believed to be prior art to the present application.

Considering the cited patent as a reference, it is respectfully submitted that the cited printed circuit board does **not** have "a corner rounded portion (reference number 6B)," as alleged by the Examiner.

In Uchikawa et al, the inner buildup wiring pattern 30a is also electrically connected to the base wiring pattern 22a through a conductor portion 6B provided in each of via holes 5B (only one shown) (see column 5, lines 49-51). That is, in Uchikawa et al, the reference number 6B is not "a corner rounded portion formed by said thermosetting resin film", as set forth in claim 2, but it is the conductor portion. Thus, Uchikawa et al do not disclose "a corner rounded portion formed by said thermosetting resin film".

Therefore, the product recited in claim 2 is patentably distinct from that of Ushikawa et al, regardless of the method steps.

In view of the rejection of claim 3 under 35 U.S.C. 102(b) as being anticipated by Petefish, cited, the claim has been amended to conform more closely to claim 2, in an effort to distinguish patentably over this reference. Petefish, too, fails to make corner rounded portion 93 obvious, no such feature being found in the product of Petefish.

Petefish discloses that "as seen in FIG. 7, the blind via 46 is plated with **a conductive material 48 that interconnects the two conductive layers 40 and 42** (column 3, lines 65-67)" and that "Any of the known plating techniques can be employed to form the plating, including electroless plating in which a copper film is formed on **the via walls** (column 4, lines 1-3)". That is, Petefish's attention is only directed to forming, on the via walls, the conductive material 48 that interconnects the two conductive layers 40 and 42. Petefish's attention is never directed to forming the metal plating layer (95) on the first and the second metal foils (82 and 87), on the inner wall of the through hole (86), on the corner rounded portion (93), and on the exposed surface (92) of the second metal foil (87), as recited in the amended claim 3. As is described on page 11, line 26, to page 12, line 14 of the specification, in the through hole 86, circulation of a plating solution is improved by the shape of the corner rounded portion (or the corner R portion) 93 so that a plating layer 95 is formed on an upper surface of the metal foil 87 at the bottom 92 of the through hole 86, on a wall surface 91 of the through hole 86, and on the corner rounded portion (or the corner R portion) 93 of the through hole 86 to thereby complete the interlayer connection.

Therefore, the product recited in claim 3 is patentably distinct from that of Ushikawa et al, regardless of the method

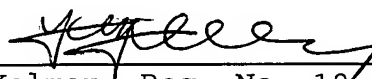
steps.

A petition for a one-month extension is attached hereto.

A sincere effort having been made to overcome all grounds of rejection, favorable reconsideration and allowance of claims 2 and 3 are respectfully solicited.

Respectfully submitted,

SHIGETOSHI ABE ET AL

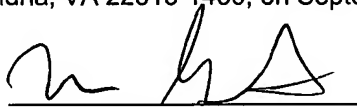


Kurt Kelman, Reg. No. 18,628
Allison C. Collard, Reg. No. 22,532
Edward R. Freedman, Reg. No. 26,048
Attorneys for Applicants

COLLARD & ROE, P.C.
1077 Northern Boulevard
Roslyn, New York 11576
(516) 365-9802

Enclosure: Request for extension
Marked-up drawings

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: MAIL STOP FEE AMENDMENT, COMMISSIONER FOR PATENTS, P.O. Box 1450, Alexandria, VA 22313-1450, on September 4, 2003.



Maria Guastella

FIG. 1A
RELATED ART

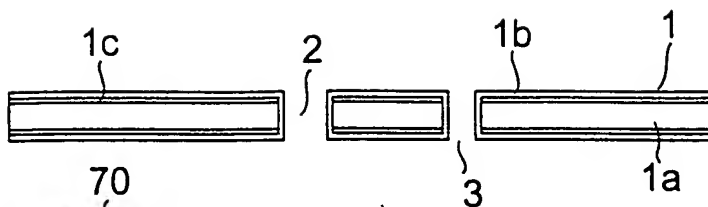


FIG. 1B
RELATED ART

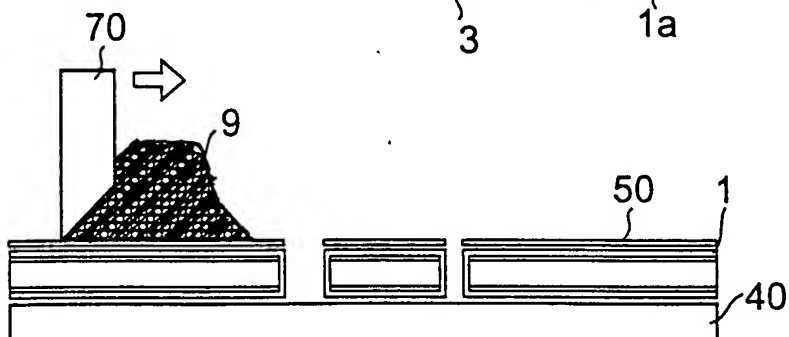


FIG. 1C
RELATED ART

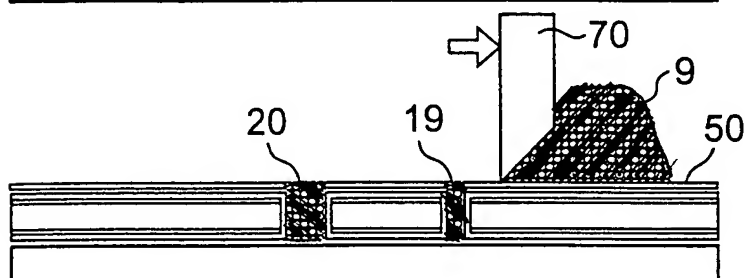


FIG. 1D
RELATED ART

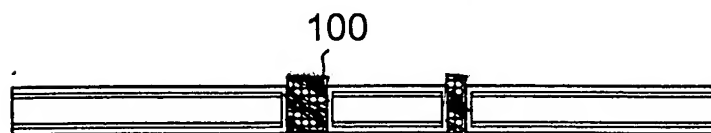


FIG. 1E
RELATED ART

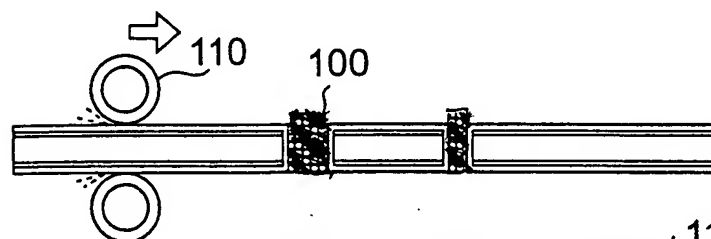


FIG. 1F
RELATED ART

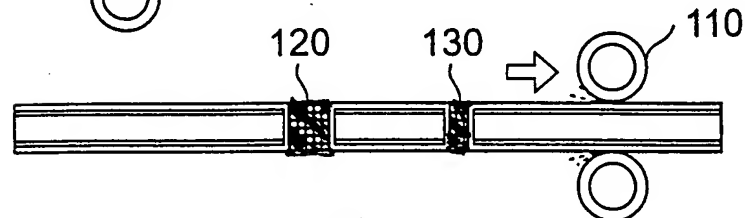


FIG. 1G
RELATED ART

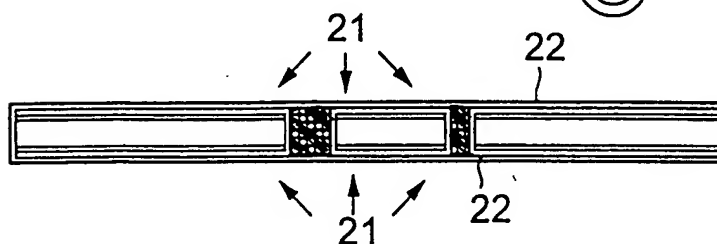




FIG. 1H
RELATED ART

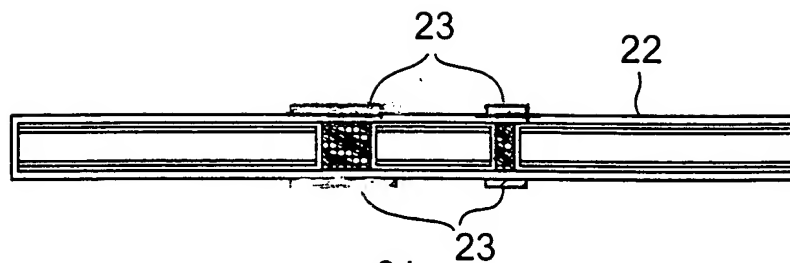


FIG. 1I
RELATED ART

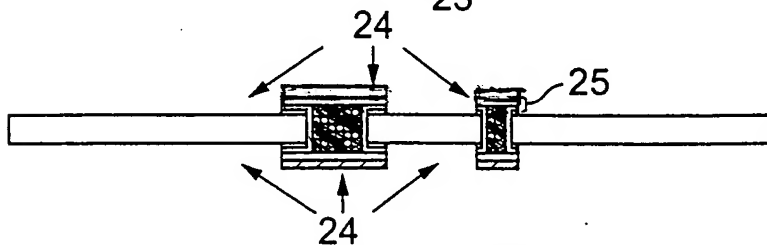
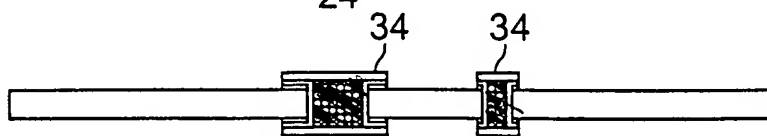


FIG. 1J
RELATED ART



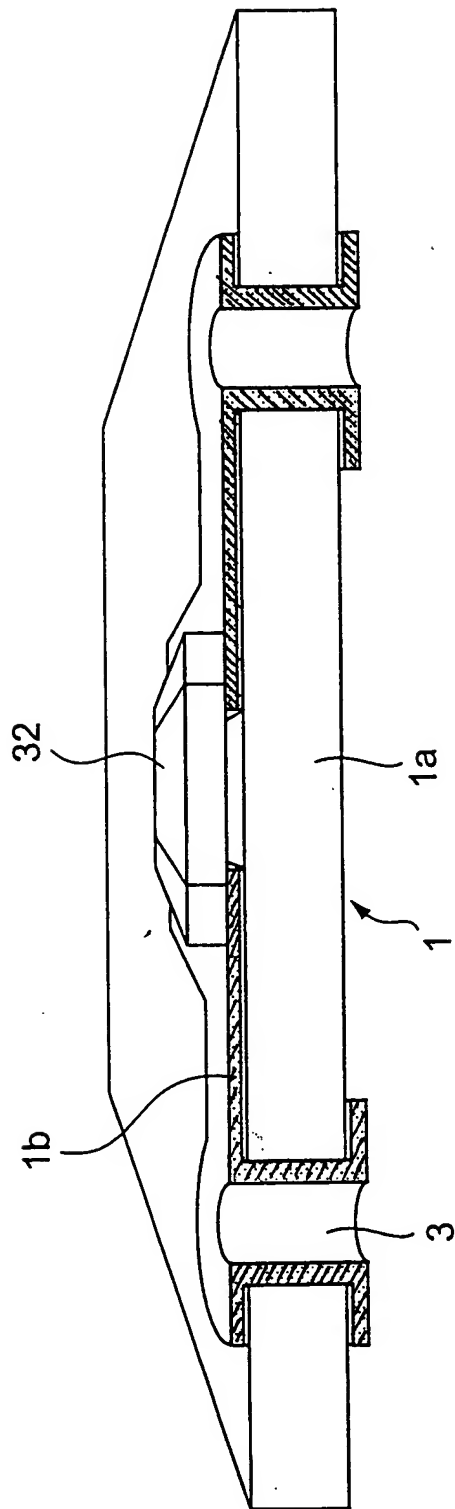


FIG. 2 RELATED ART

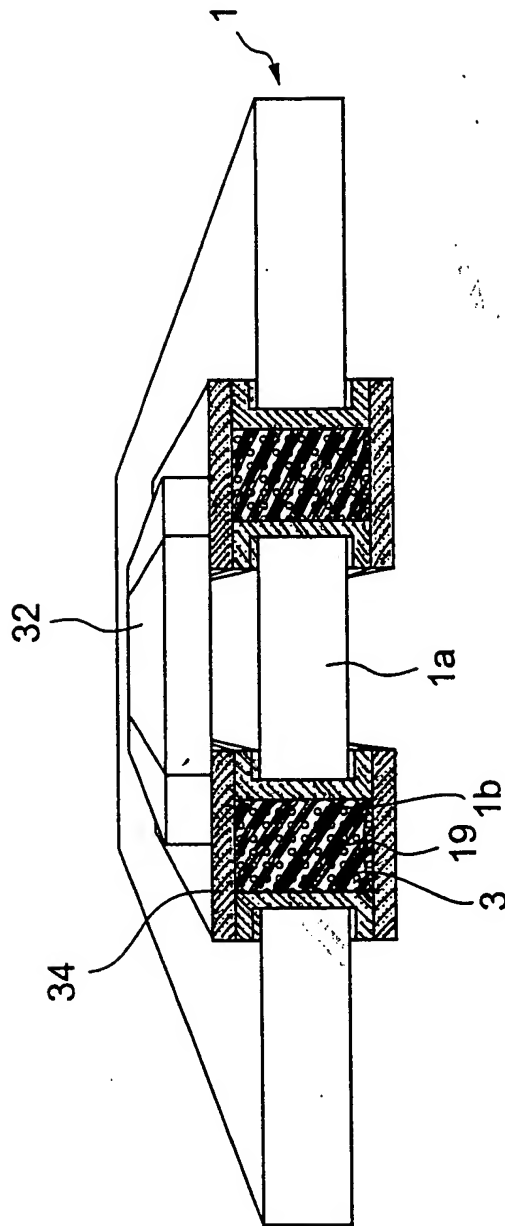


FIG. 3 RELATED ART

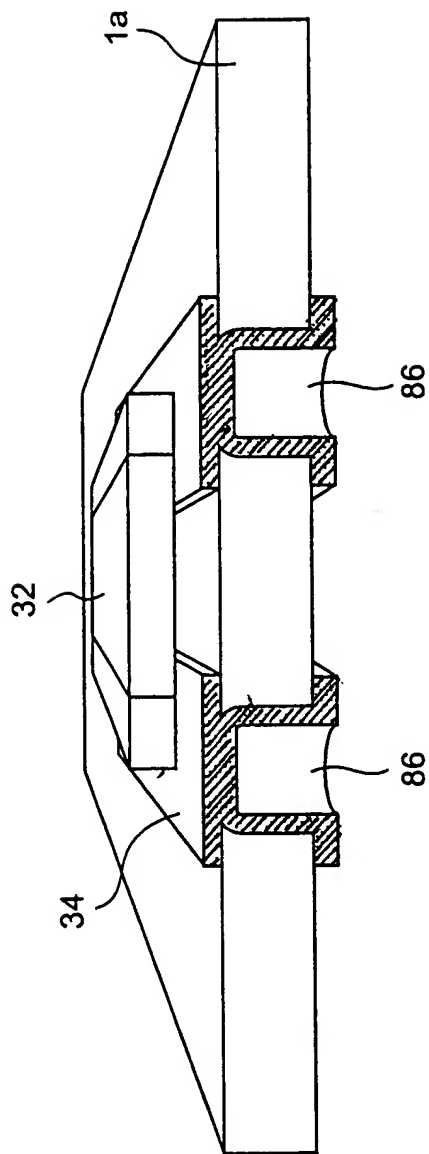


FIG. 5